SIEMENS

Course Description

Tessent

Tessent IJTAG Advanced Topics

Course Code	306732-US
Software	Tessent 2026.2
User Level	Advanced
PricingID	Contact Us
Live Online Duration	6 hours for each day for 2 days

Designing a modern product requires the integration of multiple IP blocks from both in-house and third party sources. The Siemens EDA Tessent™ IJTAG solution delivers comprehensive automation support for implementing the IEEE 1687 standard, providing plug-and-play IP test and instrumentation integration.

The Tessent™ IJTAG Advanced Topics build on your knowledge of the Instrument Connectivity Language (ICL) and the Procedural Description Language (PDL) in order learn how to perform IJTAG network insertion, and how to migrate designs that use other standards, for example IEEE1149.1 or IEEE1500, to IJTAG. It also illustrates how to use IJTAG with the different Tessent tools like ATPG, MemoryBIST, and SSN. Finally, the course explains the usage of IJTAG together with SSN to introduce High-Bandwidth IJTAG (HB-IJTAG), which is explained in detail, with its different settings, implementation, benefits, and limitations.

The chip-level PDL commands can be translated to ATE pattern formats (STIL, WGL, and so on). QuestaSim™ is used to simulate Verilog testbenches for these PDL verifications in some of the labs.

The hands-on labs are designed to reinforce key concepts through practical experience and to develop proficiency with Tessent IJTAG, and provides the basis for understanding the usage of IJTAG in the Tessent Integrated Flow under the guidance of industry-expert instructors.

The training course covers the basics that are required by Tessent MemoryBIST, Tessent ATPG with TestKompress, and Tessent SSN.

PREREQUISITES

- A basic understanding of IJTAG and SSN is helpful

PRIMARY COURSE TOPICS

What You'll Learn

- Leverage IEEE 1149.1/IEEE 1500-based test access architecture to perform IJTAG functions.
- Use Tessent IJTAG DRC syntax and semantics rules to debug your design using Tessent Visualizer.
- Create, edit, and insert IJTAG networks into design modules.
- Implement and use Tessent IJTAG in Memory BIST.
- Understand how IJTAG can be used with ATPG and SSN.
- Understand HB-IJTAG and its implementation and different settings.

Throughout this course, extensive hands-on lab exercises provide you with practical experience using Tessent software. Hands-on lab topics include:

- Create, edit, and insert an IJTAG network.
- Incorporate IEEE 1149.1 into your design.
- Create a testbench for retargeting PDL commands.

- Incorporate an IJTAG design into the Tessent MemoryBIST flow.
- Insert HB-IJTAG into different hierarchy levels of a design.