Altium Designer Design Rules & Constraint Manager

OEM: Altium

COURSE DESCRIPTION

Altium Designer Design Rules and Constraint Manager—offered as public instructor-led or private team training—shows you how to move from manually managed rules to a scalable, constraint-driven design workflow. In a dedicated Altium Workspace, you'll configure, apply, and verify electrical, high-speed, and manufacturing constraints that improve signal integrity, reduce respins, and ensure fabrication-ready PCB layouts. Configure and scope design rules for clearances, widths, vias, and net classes in the Constraint Manager Apply differential pair, length matching, and xSignal constraints to meet high-speed timing requirements Use design queries to create precise, reusable rule scopes for complex designs Define HDI via structures, DFM/DFA requirements, and creepage constraints for compliant layouts Run automated DRC to validate constraints early and eliminate rule violations before fabrication Earn an Altium certificate and digital badge to validate your constraint management expertise

AUDIENCE PROFILE

- PCB designers adopting a constraint-driven design methodology
- High-speed design engineers working with differential pairs, length matching, and xSignals
- Layout engineers responsible for signal integrity and timing closure
- Teams standardizing design rules across projects and designs
- Engineers developing HDI or manufacturing-ready PCB layouts
- Anyone looking to eliminate rule violations before fabrication

PREREQUISITES

- A stable internet connection
- Access to an Altium Account
- Latest Altium Designer installation

COURSE OBJECTIVES

By the end of this course, participants will be able to:

- This section doesn't contain any content.

COURSE OUTLINE

Module 1: Accessing the Altium Platform and Training Setup

- Accessing Altium Platform - Learn how to access the designated training workspace and connect to the Altium Platform environment
- Training Folder Structure - Navigate the training workspace, understand the project organization, and locate exercise files and reference materials
- Design Environment Preparation - Configure the Altium Designer environment and familiarize yourself with the Constraint Manager interface for the exercises to follow

Module 2: Design Rules and Net Class Management

- Default Design Rules - Understand the structure and hierarchy of Altium Designer's default design rules, including rule types, priorities, and scoping mechanisms
- Rule Configuration and Customization - Learn how to create, modify, and manage design rules for electrical clearances, trace widths, via sizes, and other critical parameters within the Constraint Manager
- Net Classes - Define and manage net classes to group related nets, enabling efficient rule application across power, signal, and high-speed net groups
- Constraint Manager Navigation - Gain hands-on experience navigating the Constraint Manager interface to view, edit, and apply constraints across the design

Module 3: Differential Pairs and Design Queries

- Differential Pairs - Define differential pair relationships, configure spacing and impedance constraints, and manage differential pair classes for high-speed signal routing
- Using Design Queries - Master the query language to create precise rule scopes, target specific nets, components, or regions, and build complex conditional rules using the Query Builder and manual query expressions
- Advanced Scoping Techniques - Combine design queries with net classes and component classes to create sophisticated, context-aware design rules

Module 4: Length Matching and xSignals

- Length Matching - Configure matched-length rules for signal groups, define tolerance constraints, and use interactive length tuning tools to achieve precise timing alignment in high-speed interfaces
- xSignals - Understand and define xSignals to represent complete signal paths through series passive components, enabling accurate length and timing analysis across net boundaries
- xSignal Configuration and Management - Create xSignal definitions from schematic and PCB, manage xSignal classes, and apply matched-length constraints to xSignal groups for interfaces such as DDR, USB, and PCIe
- Practical Length Tuning - Hands-on exercises using the interactive length tuning router to meet matched-length constraints while maintaining clean routing

Module 5: HDI Vias, Manufacturing Constraints, and Creepage

- HDI Vias - Configure via rules for HDI designs, including microvias, blind vias, buried vias, and via-in-pad strategies, with proper layer span and aspect ratio constraints
- Rules for DFM and DFA - Define Design for Manufacturing (DFM) and Design for Assembly (DFA) rules to ensure board designs meet fabrication house capabilities and assembly process requirements
- Creepage - Configure creepage and clearance constraints based on voltage ratings and safety standards (such as IPC-2221 and IEC 60950/62368), ensuring designs meet regulatory compliance requirements
- Constraint Verification and DRC - Run design rule checks to validate all configured constraints, identify and resolve violations, and prepare designs for manufacturing handoff