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Designing with the Zynq UltraScale+ RFSoC

OEM: AMD • Code: CONN-RFSOC

COURSE DESCRIPTION

This course provides an overview of the hard block capabilities for the AMD Zynq™ UltraScale+™ RFSoC family with a special emphasis on the RF Data Converter and Soft-Decision FEC blocks.

AUDIENCE PROFILE

- Hardware designers interested in understanding the architecture and capabilities of the Zynq UltraScale+ RFSoC data converter and SD-FEC hard blocks.

PREREQUISITES

- Suggested: Understanding of the Zynq UltraScale+ MPSoC architecture
- Basic familiarity with data converter terms and principles
- Basic familiarity with forward error correction terms and principles
- Vivado™ Design Suite 2026.1
- Vitis™ Unified IDE 2026.1
- Siemens® Questa Advanced Simulator (optional)
- Host computer for running the above software
- Zynq UltraScale+ RFSoC ZCU111 board* * This course focuses on the Zynq UltraScale+ RFSoC architecture. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

COURSE OBJECTIVES

By the end of this course, participants will be able to:

- Describe in general the AMD Zynq UltraScale+ RFSoC family
- Identify typical applications for the RF data converters
- Describe the architecture and functionality of the RF-ADC and RF-DAC
- Utilize the RF-ADC and RF-DAC via configuration, simulation, and implementation
- Identify the requirements and options for data converter PCB designs
- Describe the architecture and functionality of the Soft-Decision FEC hard IP
- Utilize the Soft-Decision FEC via configuration and simulation
- Utilize the DFE hard IPs

COURSE OUTLINE

Module 1: Zynq UltraScale+ RFSoC Overview

- Overview of the Zynq UltraScale+ RFSoC architecture, including brief introductions to RF, RF data converter solutions, SD-FEC solutions, driver support, and tool support.

Module 2: RF-ADC Hardware

- Covers the basics of RF-ADCs. Reviews RF-ADC architecture, functionality, interfaces, configuration, and driver support.

Module 3: RF-DAC Hardware

- Covers the basics of RF-DACs. Reviews RF-DAC architecture, functionality, interfaces, configuration, and driver support.

Module 4: RFSoC Hardware

- Provides an overview of the ZCU111 board and describes board setup.

Module 5: Data Converter Design

- Describes common features, the design flow, utilizing the example design by simulation and implementation, and verifying RF data converter functionality on real hardware. Includes practice of using a software driver to modify RF data converter parameters.

Module 6: Data Converter Practice

- Provides practical RF data converter experience using the ZCU111 board evaluation tool and RF analyzer tool. Demonstrates a PYNQ-based application to validate QPSK streams. Describes RF data converter frequency planning. Provides a design example combining hard and software components

Module 7: PCB Design for RFSoC Devices

- Describes power requirements, performing power estimation, and utilizing the power design. Analog signal requirements, PCB materials and layer stackup options, and analog trace design are also covered.

Module 8: Soft-Decision FEC Hardware

- Covers the basics of forward error correction. Reviews the SD-FEC architecture, functionality, interfaces, configuration, and driver support.

Module 9: RFSoC DFE

- Describes the RFSoC DFE series digital front-end hardened IPs. Highlights the architecture, functionality, interfaces, configuration, and usage of the DFE IP cores.