

Designing with the Versal AI Edge Series Gen 2 and Prime Series Gen 2: Architecture

OEM: AMD • Code: VER2-ARCH

COURSE DESCRIPTION

Learn about the AMD Versal™ AI Edge Series Gen 2 and Prime Series Gen 2 adaptive SoC architectures, which combine programmable logic with a new high-performance processing system and next-generation AI Engines. Also learn how these devices facilitate end-to-end acceleration and maximize system performance for embedded systems—all in a single device built on a foundation of enhanced safety and security.

AUDIENCE PROFILE

- Software and hardware developers, system architects, and anyone who wants to learn about the architecture of the Versal AI Edge Series Gen 2 and Prime Series Gen 2 devices

PREREQUISITES

- Basic knowledge of AMD FPGAs and adaptive SoCs
- Basic knowledge of the AMD Vivado™ and Vitis™ tools
- Vivado Design Suite 2026.1
- Vitis Unified IDE 2026.1
- Architecture: Versal adaptive SoC

COURSE OBJECTIVES

By the end of this course, participants will be able to:

- Describe the different compute resources available in the AMD Versal adaptive SoC
- Explain the new high-performance processing system (PS)
- Describe the next-generation AI Engine architecture
- Describe the programmable network on chip (NoC) resources
- Outline the available DDR5/LPDDR5X memory controller support
- Describe the new image and video processing hard blocks
- Explain the functional safety and security enhancements
- Identify the available PCI Express Gen 5 and 32G high-speed serial transceiver solutions

Module 1: Day 1

- Introduction and Portfolio Overview: Describes the need for Versal devices and offers an overview of the Versal portfolio.
- Architecture Overview: Provides a high-level overview of the Versal architecture, illustrating the various compute resources available in the Versal architecture.
- Design Tool Flow: Maps the various compute resources in the Versal architecture to the tools required and describes how to target them for final image assembly.
- Programmable Logic (PL): Describes the logic resources available in the programmable logic. Also discusses the clocking architecture, clock buffers, clock routing, and clock de-skewing options.
- SelectIO™ Resources: Describes the I/O bank, SelectIO interface, and I/O delay features.
- Processing System: Reviews the Arm® Cortex®-A78AE processor APU and Cortex- R52 processor RPU that form the processing system. Discusses high-speed connectivity, boot modes, system peripherals, and power domains. Also introduces the AMD Embedded Development Framework (EDF) for streamlined application development.
- Platform Management Controller (PMC): Describes the platform management controller architecture and the role of platform loader and manager (PLM) in the Versal device boot process.
- Boot and Configuration: Covers the boot phases, flows, and modes along with the process of generating a boot image. Also discusses the concept and benefits of segmented configuration.
- AIE-ML v2 Architecture Overview: Discusses the AI Engine AIE-ML v2 array architecture and its tiles. Also lists the key differences between the AIE, AIE-ML, and AIE-ML v2 architectures.

Module 2: Day 2

- AMD Vitis AI for AMD Versal AI Edge Series Gen 2 Devices: Describes the Vitis AI software stack, AI deployment flow, and NPU optimization capabilities for AMD Versal AI Edge Series Gen 2 devices.
- NoC Architecture: Covers the reasons to use the network on chip, the NoC architecture and its basic elements, design entry flows, and common terminology.
- Designing with DDR5: Describes the DDR5 memory controller features and its configuration flow. Also demonstrates how to tune a design to increase efficiency.
- Multimedia Hard Blocks: Reviews the multimedia-specific hard IP blocks such as VCU2, GPU, and ISP available in the Versal devices.
- Security and Functional Safety Overview: Describes the security architecture and the available security units. Also provides an overview of the increased embedded system security.
- PCI Express Solutions: Provides an overview of the PCIe® module and describes the PL and MDB PCIe blocks.
- Serial Transceivers: Describes the transceivers in the Versal device. Also introduces the new GT Wizard Subsystem flow.