Questa Power Aware and UPF

OEM: Siemens • Code: 288781-US

COURSE DESCRIPTION

This course will help you effectively use Visualizer™ Debug Environment with Questa Sim to perform Power Aware verification. It includes an introduction to power problems in SoCs and UPF (Unified Power Format) basics for power architecture modeling. Also, it introduces the successive refinement flow and how it works. It discusses static and dynamic checks. As well as the most commonly used windows for Power Aware debugging such as Sim (Structure), Source, Dataflow, Schematic, Variables, Wave window, PA Domains window, etc. In addition, it covers PA Coverage and how to create/manage PA test plans.

AUDIENCE PROFILE

- This section doesn't contain any content.

PREREQUISITES

- Familiarity with Questa Core/Prime and Visualzier Debug Environment.

COURSE OBJECTIVES

By the end of this course, participants will be able to:

- Discuss Power Problems in SOC
- Learn the UPF (Unified Power Format) basics for Power Architecture Modelling
- Explore Successive Refinement Flow
- Construct and Work with Constraint UPF, Configuration UPF, and Implementation UPF
- Learn the Implementation Impacts with Successive Refinement Flow
- Enable Power Aware Sim Debug
- Use the Power Aware Static and Dynamic Checks
- Explore the most commonly used windows for PA debug
- Use PA Views (Crossing, Domains, SimChecks, Liberty, States, and Supply Network)
- Create / Manage PA Testplan
- Enable PA coverage collection
- Review coverage in Visualizer GUI
- Create Questa Power Aware Coverage reports

COURSE OUTLINE

LAB OUTLINE

- Throughout this course, extensive hands-on lab exercises provide you with practical experience using Questa™ 2025.1 and Visualizer™ Debug Environment 2025.1 software. Hands-on lab topics include:
- Writing Constraint UPF
- Writing Configuration UPF
- Writing Implementation UPF
- Debugging Low Power Designs with a Visualizer
- Low Power Coverage with Visualizer