

Questa Clock Domain Crossing Verification

OEM: Siemens • Code: 304459-US

COURSE DESCRIPTION

This course is for design and verification engineers that need to understand how to address the challenges asynchronous clocks pose on their verification methodology. The course will cover the methodology required to run structural analysis to pinpoint potential synchronization issues between clock domains, dynamic checking with assertions of CDC protocols, and how to perform metastability effects modeling in simulation to find intricate clock domain crossing bugs.

AUDIENCE PROFILE

- This section doesn't contain any content.

PREREQUISITES

- This section doesn't contain any content.

COURSE OBJECTIVES

By the end of this course, participants will be able to:

- Develop a methodology for CDC verification

Utilize static analysis to check that synchronizers exist and are connected properly at the clock domain boundaries of a design

- Compile and analyze Verilog and VHDL RTL designs
- Use the graphical CDC debug environment

Use automatically generated assertions to check that CDC signals are being driven with the correct protocol in simulation

- Compile and run assertions in simulation
- Debug simulation failures
- View CDC coverage

Add metastability effects modeling to your simulation

- Debug simulation failures
- View metastability effects coverage

