

Programming Zynq SoCs with MATLAB and Simulink

OEM: MathWorks • Code: MW-PROGRAMMING-XILINX-ZYNQ-SOCS-WITH-MAT

COURSE DESCRIPTION

This hands-on, two-day course focuses on developing and configuring models in Simulink® and deploying on Zynq®-7000 All Programmable SoCs. The course is designed for Simulink users who intend to generate, validate, and deploy embedded code and HDL code for software/hardware codesign using Embedded Coder® and HDL Coder™.

A ZedBoard™ is provided to each attendee for use throughout the course. The board is programmed during the class.

Zynq platform overview and environment setup
 Introduction to Embedded Coder and HDL Coder IP core generation and deployment
 Using AXI4 interface
 Processor-in-the-loop verification
 Data interface with real-time application
 Integrating device drivers
 Custom reference design

AUDIENCE PROFILE

- IT professionals and technical staff seeking hands-on training in this course's subject area.

PREREQUISITES

- Simulink Fundamentals (or Simulink Fundamentals for Automotive Applications or Simulink Fundamentals for Aerospace Applications)
- Knowledge of C and HDL programming languages

COURSE OBJECTIVES

By the end of this course, participants will be able to:

- Configure Zynq-7000 platform and MATLAB environment.
- Configure Simulink models for embedded code generation and effectively interpret the generated code.
- Use HDL Workflow Advisor to configure a Simulink model, generate and build both HDL and C code, and deploy to Zynq platform.
- Use various AXI interfaces for data communication between processing system and programmable logic.
- Use processor-in-the-loop to verify the algorithm running on Zynq platform and profile the execution times in your production algorithm.
- Use the UDP interface to stream data between Simulink and the real-time application running on Zynq platform.
- Develop device driver interfaces for integrating peripherals on processing system.
- Create and package reusable IP for Vivado and register custom boards and reference designs.

Module 1: Day 1 of 2

Zynq Platform Overview and Environment Setup

- Zynq-7000 overview
- Setting up Zynq platform and software
- Configuring MATLAB environment
- Testing connectivity to Zynq hardware

Introduction to Embedded Coder and HDL Coder

- Architecture of an embedded application
- Generating ERT code
- Code modules
- Data structures in generated code
- Configuring a Simulink model for HDL code generation
- Using HDL Workflow Advisor

IP Core Generation and Deployment

- Configuring a subsystem for programmable logic
- Configuring the target interface and peripherals
- Generating the IP core and integrating with SDK
- Building and deploying the FPGA bitstream
- Generating and deploying a software interface model
- Tuning parameters with External Mode

Using AXI4 Interface

- AXI interface overview
- AXI4-Lite applications
- Using AXI4-Stream
- AXI4 performance considerations

Processor-in-the-Loop Verification

- Processor-in-the-loop (PIL) workflow on Zynq
- PIL verification with model reference
- Code execution profiling with PIL
- PIL considerations

Module 2: Day 2 of 2

Data Interface with Real-Time Application

- Data interface overview
- Configuring UDP blocks for data streaming

- Synchronizing data between Simulink and Zynq
- Data interface with AXI Stream
- Design partitioning
- Data interface considerations

Integrating Device Drivers

- Workflow for developing device drivers
- Using the Legacy Code Tool
- GPIO interface
- Cross-compiling device drivers

Custom Reference Design

- Motivations for a custom reference design
- Creating reusable IP for Vivado
- Reference design overview
- Customizing a reference design
- Registering board and custom reference design