Programming Zynq RFSoCs Using Simulink

OEM: MathWorks • Code: MW-PROGRAMMING-ZYNQ-RFSOCS-USING-SIMULIN

COURSE DESCRIPTION

This hands-on, two-day course focuses on developing and configuring models in Simulink® and deploying on Zynq® UltraScale+ RFSoCs. Zynq RFSoC platform overview and environment setup Frequency planning and Nyquist zones System simulation, deployment and testing of the RFSoC with the SoC Blockset Deployment via HW/SW co-design

AUDIENCE PROFILE

- IT professionals and technical staff seeking hands-on training in this course's subject area.

PREREQUISITES

- Knowledge of concepts of communication systems and hardware design.

COURSE OBJECTIVES

By the end of this course, participants will be able to:

- Introduction to RFSoC's device settings, parameters, and hardware details
- Provide an introduction to frequency planning with Nyquist zones and sampling rates as used with the DAC and ADC tiles in the RFSoC
- Simulate transmission and reception of a digital signal in the RFSoC
- Simulate, model and perform analysis of SoC HW/SW architectures specifically to target gen 1,3 RFSoC.
- Deploy and interact with your HDL IP design at run-time verify performance from MATLAB

COURSE OUTLINE

Module 1: Day 1 of 2

RFSoC Device Overview

- Introducing Zynq RFSoC._
- Reviewing RFSoC transceiver tiles.
- Examining RFSoc digital up converter and down converter.
- Reviewing differences between RFSoC Generation 1 and Generation 3 devices.

- Reviewing the support offerings of MathWorks for RFSoC.

Frequency Planning

- Using the DAC tile Digital Quadrature Modulator for digital up conversion
- Using the normal mode (Nyquist Zone 1) and mixed mode (Nyquist Zone 2) operations of DAC tiles for transmission
- Applying a bandpass sampling theorem to choose a sampling rate for the receiver

Getting the model ready for the RFSoC

- Review frame-based processing
- Simulate a transmitter and receiver model for the RFSoC
- Prepare model for deployment to the RFSoC

Module 2: Day 2 of 2

Target RFSoC using SoC Blockset

- Introduction to SoC Blockset
- Use RFSoC template from SoC Blockset to create RFSoC system modeling framework
- Simulate and generate code for PL and PS side of algorithm using SoC Builder
- Deploy application on the board targeting FPGA, ARM and RF converter tiles

Hardware Software Co-design for RFSoC

- Generate and examine the RFSoC Vivado project
- Access streaming and parameter data of the generated HDL IP at run-time
- Dynamically configure RF Data Converter settings in MATLAB