DSP for FPGAs

OEM: MathWorks • Duration: 3 Days (24 hrs) • Code: MW-DSP-FOR-FPGAS

COURSE MODULES & TOPICS

Day 1 of 3

Introduction to DSP FPGA Hardware

- From discrete logic to FPGAs -some history!
- The generic DSP system
- DSP cores and processors review
- Custom and semi-custom ASICs
- System-on-chip (SOC)
- FPGA flexibility and functionality
- FPGAs vs Programmable DSPs

FPGA Fundamental Concepts

- Timing and critical path issues
- Pipelining
- Arithmetic implementation: multiply and add
- Parallel and serial implementations
- FIR Filters

FPGA Technology

- The FPGA technology roadmap
- Clocking rates, data rates, and sample rates
- FPGA memory and registers
- Input/output blocks and requirements
- Bits, Slices, and Configurable Logic Blocks
- FPGA Families

DSP Arithmetic Essentials

- 2's complement fixed point arithmetic
- Full adders and multiplier cells
- Division and square root implementation
- Wordlength issues and Fixed point arithmetic
- Saturate and wraparound
- Overflow and underflow

Signal Flow Graph (SFG) Techniques

- DSP/Digital Filter Signal Flow Graphs
- Latency, delays, and "anti-delays"
- Re-timing: Cut-set and delay scaling
- The transpose FIR
- Pipelining and multichannel architectures
- SFG topologies for FPGAs

Digital Filtering

- Low pass, high pass, band pass, and band stop
- FIR, IIR, Adaptive
- Impulse Response
- Frequency Response

Day 2 of 3

Recursive DSP Retiming (IIR and LMS)

- IIR
- Adaptive LMS
- Non-Canonical LMS

Serial Filter Implementation

- Serial filters
- Serial-parallel filters
- Hardware cost

Multi-Channel Filter Implementation

- Cut set retiming
- Delay scaling rule
- Implementation issues
- Extending serial filters to multiple channels

Frequency Domain Processing

- DFT, FFT and IFFT
- FFT FPGA architectures
- FFT wordlength growth and accuracy

Multirate Signal Processing for FPGAs

- Upsampling and interpolation filters
- Downsampling and decimation filters
- Efficient arithmetic for FIR implementation
- Integrators and differentiators
- Half-band, moving average and comb filters

- Cascade Integrator Comb (CIC) Filters (Hogenauer)
- Efficient arithmetic for IIR Filtering

Day 3 of 3

CORDIC Techniques

- CORDIC rotation mode and vector mode
- Compute cosine and sine function
- Compute vector magnitude and angle
- Architecture for FPGA implementation

Adaptive DSP Algorithms and Applications

- Adaptive applications (equalization, beamforming)
- LMS Algorithms and parallel implementation
- Non-canonical LMS algorithms
- Linear algebra; solving linear systems of equations
- The QR algorithm for adaptive signal processing
- QR processing requirements and numerical issues

Numerically Controlled Oscillators

- IIR filters
- CORDIC rotations
- Lookup Tables
- Evaluate spectral purity and SFDR

Timing and Synchronization Issues

- Carrier recovery, squaring and Costas loops, PLLs
- Phase rotations; Sampling rate conversions
- Symbol timing recovery, early/late gate detection
- Delay locked loop timing and synchronization